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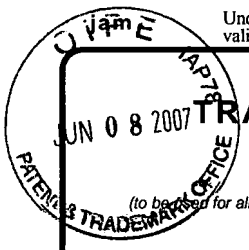

TRANSMITTAL FORM

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Application / Conf. No.	09/765,907 / 9367
Filing Date	January 19, 2001
First Named Inventor	Stephen M. Trimberger
Examiner Name	Carl G. Colin
Art Unit	2136
Patent No.	
Attorney Docket Number	X-714 US

ENCLOSURES *(check all that apply)*

- [X] Fee Transmittal Form
- [ ] Amendment / Reply
  - [ ] Preliminary Amendment
  - [ ] After Final
  - [ ] Affidavit(s)/declaration(s)
- [ ] Extension of Time Request
- [ ] Change Status to LARGE ENTITY
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Substitute PTO-1449(s) IDS by Applicant (PTO/SB/08A)
- [ ] Certified Copy of Priority Document(s)
- [ ] Response to Missing Parts/ Incomplete Application
  - [ ] Response to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Assignment Papers (with Recordation Cover Sheet)
- [ ] Declaration / Oath
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition -
- [ ] To Convert a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] After Allowance Communication to
- [X] Appeal Communication to Board of Appeals and Interferences
- [ ] Appeal Communication to Group *(Appeal Notice, Brief, Reply Brief)*
- [ ] Status Letter
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Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm or Customer Number Attn:	Michael R. Hardaway	24309 *(Customer Number)*	Reg. Number 52,992
Signature			
Date	June 6, 2007	Charge any additional fees required/credit any overpayment to our Deposit Account Number:	24-0040

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FEE TRANSMITTAL for FY 2007

Patent fees are subject to annual revision

TOTAL AMOUNT OF PAYMENT ($) 500.00

Complete if Known	
Application / Conf. No.	09/765,907 / 9367
Filing Date	January 19, 2001
First Named Inventor	Stephen M. Trimberger
Examiner Name	Carl G. Colin
Art Unit	2136
Attorney Docket No.	X-714 US

METHOD OF PAYMENT (check one)

1. [X] The Commissioner is hereby authorized to charge indicated fees, any additional fees required, and credit any over payments to:

[X] Deposit Account

Deposit Account Number: 24-0040

Deposit Account Name: XILINX, INC.

FEE CALCULATION

1. BASIC FILING FEE

Large Entity Fee Code	Fee ($)	Fee Description	Fee Paid
1001	770	Utility filing fee	
1002	330	Design filing fee	
1003	510	Plant filing fee	
1004	790	Reissue filing fee	
105	160	Provisional filing fee	

SUBTOTAL (1) ($)

2. EXTRA CLAIM FEES FOR UTILITY AND REISSUE

		Extra		Fee from below	=	Fee Paid
Total Claims	-20** =		X		=	
Indep. Claims	- 3** =		X		=	
Multiple Dependent Claims			X		=	

**or number previously paid, if greater; For Reissues, see below

Large Entity Fee Code	Fee ($)	Fee Description
1202	18	Claims in excess of 20
1201	86	Independent claims in excess of 3
1203	290	Multiple dependent claim, if not paid
1204	86	**Reissue independent claims over original patent
1205	18	**Reissue claims in excess of 20 and over original patent

SUBTOTAL (2) ($)

FEE CALCULATION (continued)

3. ADDITIONAL FEES

Large Entity Fee Code	Fee ($)	Fee Description	Fee Paid
1051	130	Surcharge - late filing fee or oath	
1052	50	Surcharge - late provisional filing fee or cover sheet.	
1812	2,520	For filing a request for exparte reexamination	
1804	920*	Requesting publication of SIR prior to Examiner action	
1805	1,840*	Requesting publication of SIR after Examiner action	
1251	120	Extension for reply within first month	
1252	450	Extension for reply within second month	
1253	1020	Extension for reply within third month	
1254	1,530	Extension for reply within fourth month	
1255	2,080	Extension for reply within fifth month	
1401	500	Notice of Appeal	
1402	500	Filing a brief in support of an appeal	$500
1403	1000	Request for oral hearing	
1451	1,510	Petition to institute a public use proceeding	
1452	110	Petition to revive - unavoidable	
1453	1,500	Petition to revive - unintentional	
1501	1,400	Utility issue fee (or reissue)	
1460	130	Petitions to the Commissioner	
1807	50	Petitions related to provisional applications	
1806	180	Submission of Information Disclosure Stmt	
8021	40	Recording each patent assignment per property (times number of properties)	
1809	790	Filing a submission after final rejection (37 CFR 1.129(a))	
1810	790	For each additional invention to be examined (37 CFR 1.129(b))	
1801	790	Request for Continued Examination (RCE)	

Other fee (specify) _____

*Reduced by Basic Filing Fee Paid **SUBTOTAL (3)** ($) 500.00

SUBMITTED BY

Complete (if applicable)

Name (Print/Type)	Michael R. Hardaway	Registration No. (Attorney/Agent)	52,992	Telephone	408-879-6149
Signature				Date	06-06-2007

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IN THE UNITED STATES PATENT OFFICE

Appellant: Stephen M. Trimberger
Assignee: Xilinx, Inc.
Title: "Copy Protection Without Non-Volatile Memory"

Ser. No.:	09/765,907	File Date:	January 19, 2001
Examiner:	Carl G. Colin	Art Unit:	2136
Docket No.:	X-714 US	Conf. No.:	9367

Board of Patent Appeals and Interferences
United States Patent and Trademark Office
P.O. Box 1450
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APPEAL BRIEF

Sir:

This is an Appeal Brief submitted pursuant to 37 C.F.R. § 41.37 for the above-referenced patent application.

I. Real Party in Interest

The real party in interest is XILINX, Inc. The above referenced patent application is assigned to XILINX, Inc.

II. Related Appeals and Interferences

Appellant is unaware of any related appeals, interferences or judicial proceedings.

III. Status of Claims

Claims 1-4, 7, 12-13, 15, 21, and 44 are rejected and are presented for appeal. Claims 5-6, 8-11, 14, 16-20, and 22–43 are cancelled. The appealed claims are in the attached Appendix of Appealed Claims.

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IV. Status of Amendments

No amendment has been filed after the Final Rejection.

V. Summary of Claimed Subject Matter

In the embodiment set forth in claim 1, the invention provides a method of securing communication of configuration data between a field programmable gate array (FPGA) and an external storage device, the method comprises counting a first number of oscillations of a first oscillator on the FPGA during a predetermined time interval (FIG. 6, #62, #66; [0030], [0031]). A second number of oscillations of a second oscillator on the FPGA is also counted during the predetermined time interval (FIG. 6, #64, #66; [0030], [0031]). A ratio between the first number and second number of oscillations is generated. The ratio is a fingerprint that represents an inherent manufacturing process characteristic unique to the FPGA (FIG. 6, #66; [0031]). Encrypted configuration data is transmitted from the storage device to the FPGA (FIG. 2, #26; [0022]). The encrypted configuration data is decrypted in the FPGA using the fingerprint as a decryption key to extract the configuration data (FIG. 2, #28; [0023]).

In another embodiment as found in claim 12, a field programmable gate array (FPGA) is provided. The FPGA comprises a plurality of configurable logic elements being programmable with configuration data to implement a desired circuit design (FIG. 1, #12; [0018]). A fingerprint element on the FPGA generates a fingerprint representing inherent manufacturing process variations unique to the FPGA (FIG. 1, #18; [0018]). The fingerprint element includes first and second oscillators (FIG. 6, #62, #64; [0031]) and a sensing circuit (FIG. 6, #66; [0031]). The sensing circuit includes means for counting a first number of oscillations of the first oscillator and counting a second number of oscillations of the second oscillator during a predetermined time interval [FIG. 6, #66; 0031] and means for generating a fingerprint as a ratio between the first number and second number of oscillations [FIG. 6, #66; 0031]. The FPGA further comprises a decryption circuit (FIG. 1, #16; [0018], [0019]) coupled to receive encrypted configuration data. The decryption circuit is configured to decrypt the

encrypted configuration data using the fingerprint as a decryption key to extract the configuration data.

In the embodiment set forth in claim 7, the first and second oscillators comprise configurable logic blocks of the FPGA (FIG. 1, #18; FIG. 6, #62, #64; [0031]).

In the embodiment set forth in claim 44, the generating of the ratio includes dividing the first number of oscillations by the second number of oscillations ([0031]).

VI. Grounds of Rejection

Claims 1-4, 7, 12-13, 15, 21, and 44 stand rejected under 35 U.S.C. §103(a) as being unpatentable over "Erickson" (U.S. Patent No. 5,970,142 to Erickson) in view of "IBM-RNG" (IBM Technical Disclosure Bulletin "Integrated Circuit Compatible Random Number Generator").

VII. Argument

The rejection of claims 1-4, 7, 12-13, 15, 21, and 44 should be reversed because the Examiner has not established a *prima facie* case of obviousness under 35 U.S.C. §103(a) over the Erickson-IBM-RNG combination.

The Examiner has failed to establish a *prima facie* case of obviousness of claims 1-4, 7, 12-13, 15, 21, and 44 over the Erickson-IBM-RNG combination because all the limitations have not been shown to be suggested by the combination.

Claims 1, 2, 3, 4, 12, 13, 15

Claim 1 includes limitations of counting a first number of oscillations of a first oscillator on the FPGA during a predetermined time interval; counting a second number of oscillations of a second oscillator on the FPGA during the predetermined time interval; and generating a ratio between the first number and second number of oscillations, wherein the ratio is a fingerprint that represents an inherent manufacturing process characteristic unique to the FPGA. These limitations are not suggested by either of Erickson or IBM-RNG.

The clear teachings of IBM-RNG do not suggest the counting of the first and second numbers of oscillations for first and second oscillators. IBM-RNG's figure shows two ring oscillators 2 and 4 and only a single divide-by-N counter for oscillator 2. For the second oscillator 4, the clock port of the divide-by-2 stage flip-flop #6 is connected to the second oscillator, and the not-Q data port of the flip-flop #6 is connected to the flip-flop 6 data-in port. IBM-RNG's description states, "The purpose of the divide-by-two stage 6 between the high frequency oscillator 4 and the sampling flip-flip 8 is to obtain a 50% duty cycle at the sample input to avoid biased outputs." IBM-RNG's description further states, "Bias can be further reduced by passing the sampling flip-flop output through the Exclusive OR 10 and latch 12." (p. 334-335; the accuracy of the page citation could not be verified because no page numbers are present on the PTO-provided IBM-RNG document) Those skilled in the art will recognize that the output of IBM-RNG's second oscillator 4 is sampled, which is clearly not suggestive of counting the number of oscillations. Thus, IBM-RNG's figure and description clearly describe a random number generator in which the number of oscillations is counted for only one oscillator, and that count is used to sample the second oscillator.

Since IBM-RNG does not count the numbers of oscillations of first and second oscillators, IBM-RNG does not suggest the limitations of generating a ratio between the first number and second number of oscillations. Furthermore, not only does IBM-RNG fail to suggest generating the ratio of two oscillator counts and using the ratio as a fingerprint, but the teachings of IBM-RNG teach away from the use of the ratio as a fingerprint. As explained in paragraphs [0030] and [0031] of the present application the two oscillator counts and the ratio between the counts may be used to avoid fingerprint drift. In contrast, IBM-RNG's approach seeks to generate non-deterministic random binary numbers. IBM-RNG's approach seeks to "only use the jitter oscillator output as a seed for a pseudo-random shift register, which is capable of high statistical quality" in order to avoid the deterministic qualities of a conventional feedback shift register approach, from which "it is possible to predict future or past results once the structure of the device and one output are known." Thus, the claimed use of the ratio of oscillator counts is clearly not suggested by IBM-RNG since the claimed ratio is for

avoiding fingerprint drift, as compared to IBM-RNG's sampling that seeks to make a key value unpredictable.

Claims 2-4 depend from claim 1, and the limitations are not shown to be suggested for the reasons set forth above.

Independent claim 12 is directed to an FPGA and includes functional limitations similar to those discussed above in regards to claim 1. Thus, the limitations of claim 12 have not been shown to be suggested by the Erickson-IBM-RNG combination.

Claims 13 and 15 depend from claim 12, and the Examiner has not shown that the Erickson-IBM-RNG combination suggests the limitations of these claims for the reasons set forth for claim 12.

Appellant respectfully submits that the Examiner has not established a *prima facie* case of obviousness for claims 1, 2, 3, 4, 12, 13, 15 because he has not shown that all the limitations of the claims are shown or suggested by the Erickson-IBM-RNG combination.

Claims 7 and 21

Claim 7 depends from claim 1, and the Erickson-IBM-RNG combination neither shows nor suggests all the limitations of claim 1 as explained above. Furthermore, the Examiner has not shown that the limitations of claim 7 are suggested by the Erickson-IBM-RNG combination. Claim 7 includes the limitations that the first and second oscillators comprise configurable logic blocks of the FPGA.

IBM-RNG does not mention configurable logic blocks of the FPGA. IBM-RNG generally states, "The two-oscillator, or jitter oscillator, approach is of interest because it can be constructed entirely of standard logic circuits." IBM-RNG's figures shows standard logic circuits such as inverters, flip-flops, XOR logic gates, a multiplexer, and a feedback shift register. Beyond these logic elements there is no apparent suggestion of using configurable logic blocks of the FPGA. Also, there is no specific suggestion of the first and second oscillators comprising configurable logic blocks of the FPGA. Therefore, it is respectfully submitted that IBM-RNG does not suggest the limitations of claim 7.

Claim 21 depends from claim 12 and includes limitations similar to those of claim 7. Thus, the Examiner has not shown that the Erickson-IBM-RNG combination suggests the limitations of claim 21 for the reasons set forth above.

Appellant respectfully submits that the Examiner has not established a *prima facie* case of obviousness for claims 7 and 21 because he has not shown that all the limitations of the claims are shown or suggested by the Erickson-IBM-RNG combination.

Claim 44

Claim 44 depends from claim 1, and the Erickson-IBM-RNG combination neither shows nor suggests all the limitations of claim 1 as explained above. Furthermore, the Examiner has not shown that the limitations of claim 44 are suggested by the Erickson-IBM-RNG combination. Claim 44 includes the limitations of the generating of the ratio including dividing the first number of oscillations by the second number of oscillations.

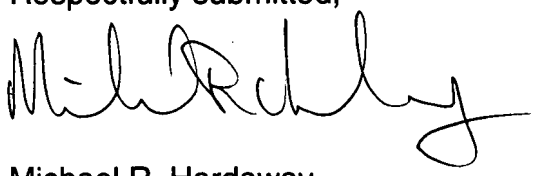
As explained above in regards to claim 1, IBM-RNG does not suggest the counting of the numbers of oscillations of two oscillators. Thus, for claim 44, IBM-RNG could neither teach nor suggest the claimed dividing of the first number of oscillations by the second number of oscillations. Therefore, the Examiner has not shown that the Erickson-IBM-RNG combination suggests the limitations of claim 44.

Appellant respectfully submits that the Examiner has not established a *prima facie* case of obviousness for claim 44 because he has not shown that all the limitations of the claims are shown or suggested by the Erickson-IBM-RNG combination.

VIII. Conclusion

In view of the above, Appellant submits that the rejections are improper, the claimed invention is patentable, and that the rejections of claims 1-4, 7, 12-13, 15, 21, and 44 should be reversed. Appellant respectfully requests reversal of the rejections as applied to the appealed claims and allowance of the entire application.

Respectfully submitted,



Michael R. Hardaway
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Reg. No. 52,992

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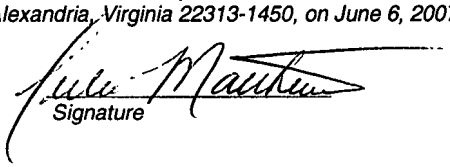
Julie Matthews
Name



Signature

APPENDIX OF APPEALED CLAIMS FOR

APPLICATION NO. 09/765,907

1. A method of securing communication of configuration data between a field programmable gate array (FPGA) and an external storage device, the method comprising:

counting a first number of oscillations of a first oscillator on the FPGA during a predetermined time interval;

counting a second number of oscillations of a second oscillator on the FPGA during the predetermined time interval;

generating a ratio between the first number and second number of oscillations, wherein the ratio is a fingerprint that represents an inherent manufacturing process characteristic unique to the FPGA;

transmitting encrypted configuration data from the storage device to the FPGA; and

decrypting the encrypted configuration data in the FPGA using the fingerprint as a decryption key to extract the configuration data.

2. The method of Claim 1, further comprising:

configuring the FPGA using the configuration data.

3. The method of Claim 2, further comprising:

transmitting the fingerprint from the FPGA to an encryption circuit;

encrypting the configuration data using the fingerprint as an encryption key; and

storing the encrypted configuration data in the storage device.

4. The method of Claim 1, wherein the fingerprint is generated during power-up of the FPGA.

7. The method of Claim 1, wherein the first and second oscillators comprise configurable logic blocks of the FPGA.

12. A field programmable gate array (FPGA), comprising:

a plurality of configurable logic elements being programmable with configuration data to implement a desired circuit design;

a fingerprint element for generating a fingerprint representing inherent manufacturing process variations unique to the FPGA, wherein the fingerprint element includes,

first and second oscillators; and

a sensing circuit including,

means for counting a first number of oscillations of the first oscillator and counting a second number of oscillations of the second oscillator during a predetermined time interval;

means for generating a fingerprint as a ratio between the first number and second number of oscillations; and

a decryption circuit coupled to receive encrypted configuration data, the decryption circuit configured to decrypt the encrypted configuration data using the fingerprint as a decryption key to extract the configuration data.

13. The FPGA of Claim 12, further comprising:

a configuration circuit for configuring the configurable logic elements with the configuration data.

15. The FPGA of Claim 12, wherein the configuration data is encrypted using the fingerprint as an encryption key to generate the encrypted configuration data.

21. The FPGA of Claim 12, wherein the first and second oscillators comprise configurable logic blocks.

44. The method of claim 1, wherein the generating the ratio includes dividing the first number of oscillations by the second number of oscillations.

APPENDIX OF EVIDENCE FOR

APPLICATION NO. 09/765,907

Appellant is unaware of any evidence submitted in this application pursuant to 37 C.F.R. §§ 1.130, 1.131, and 1.132.

APPENDIX OF RELATED PROCEEDINGS FOR APPLICATION NO. 09/765,907

Appellant is unaware of any related appeals, interferences or judicial proceedings.